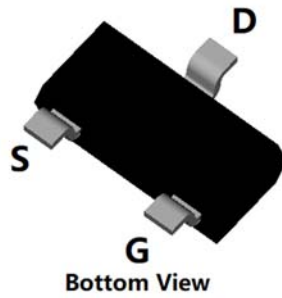
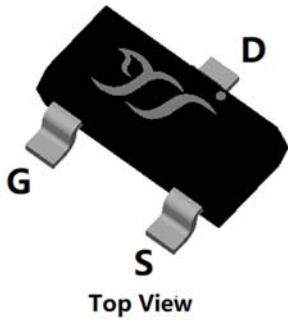
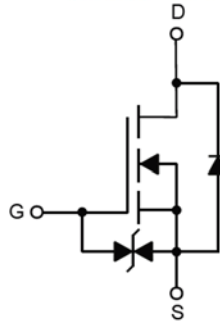


## N-Channel Enhancement Mode Field Effect Transistor



**SOT-23**



### Product Summary

- $V_{DS}$  60V
- $I_D$  300mA
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) <2.0ohm
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) <2.5ohm
- ESD protected up to 2.0KV (HBM)

### General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface: TTL/CMOS
- 12V, 24V Automotive systems

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	60	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current @ $T_A=25^\circ C$	$I_D$	300	mA
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	1.5	A
Total Power Dissipation @ $T_A=25^\circ C$	$P_D$	520	mW
Thermal Resistance Junction-to-Ambient @ Steady State <sup>B</sup>	$R_{\theta JA}$	285	$^\circ C/W$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+175	$^\circ C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
2N7002KDHQ	F2	72KD.	3000	30000	120000	7" reel



# 2N7002KDHQ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±10	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.1	1.5	2.4	V
Static Drain-Source On-Resistance	R <sub>Ds(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =300mA		1.1	2.0	Ω
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =200mA		1.3	2.5	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =115mA, V <sub>GS</sub> =0V		0.9	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz		150		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		25		pF
Output Capacitance	C <sub>oss</sub>			8		
Reverse Transfer Capacitance	C <sub>rss</sub>			4		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =1A		1.75		nC
Gate Source Charge	Q <sub>gs</sub>			1.00		
Gate Drain Charge	Q <sub>gd</sub>			0.25		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>SD</sub> =1A, di/dt=100A/us		3.9		nC
Reverse Recovery Time	t <sub>rr</sub>			15		ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =1A, R <sub>g</sub> =3Ω		4.6		ns
Turn-on Rise Time	t <sub>r</sub>			20.0		
Turn-off Delay Time	t <sub>D(off)</sub>			10.5		
Turn-off Fall Time	t <sub>f</sub>			25.5		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. The value of R<sub>θJA</sub> is measured with the device mounted on the minimum recommend pad size, in the still air environment with T<sub>A</sub>=25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.



# 2N7002KDHQ

## ■ Typical Performance Characteristics

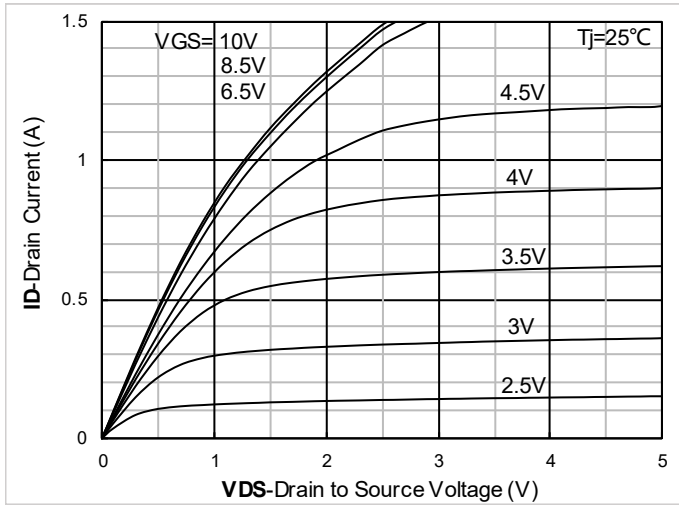


Figure1. Output Characteristics

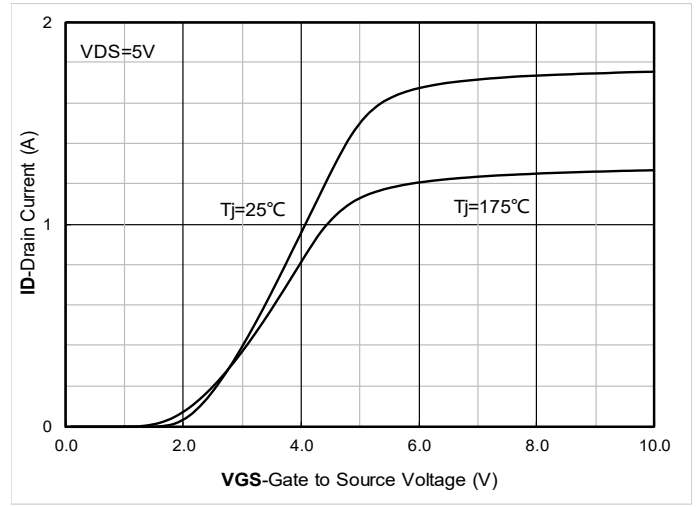


Figure2. Transfer Characteristics

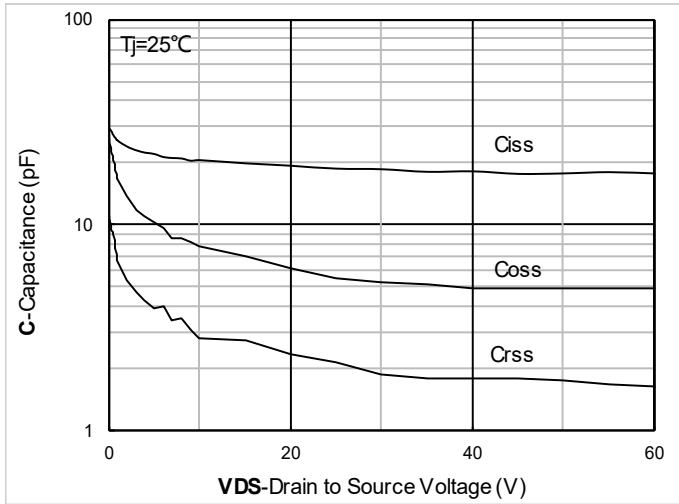


Figure3. Capacitance Characteristics

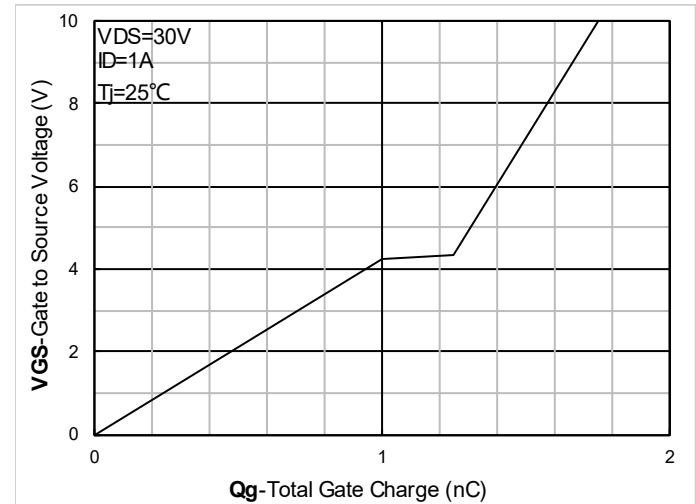


Figure4. Gate Charge

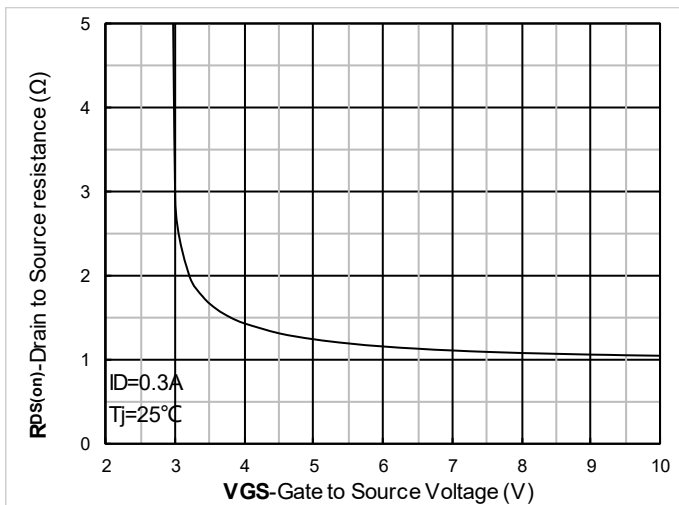


Figure5. On-Resistance vs Gate to Source Voltage

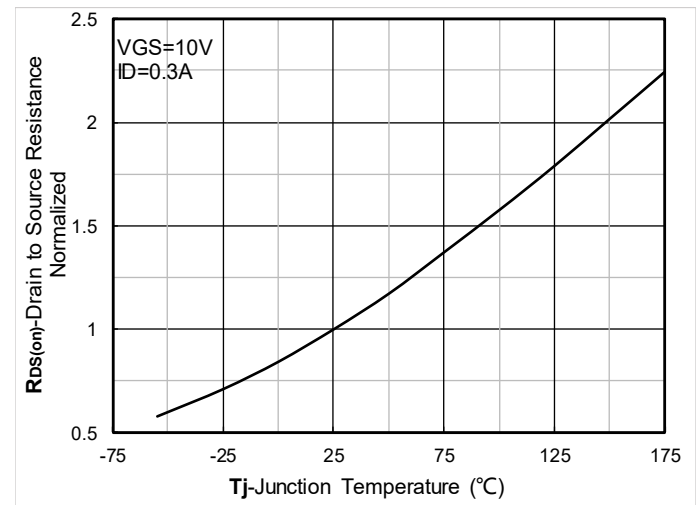


Figure6. Normalized On-Resistance



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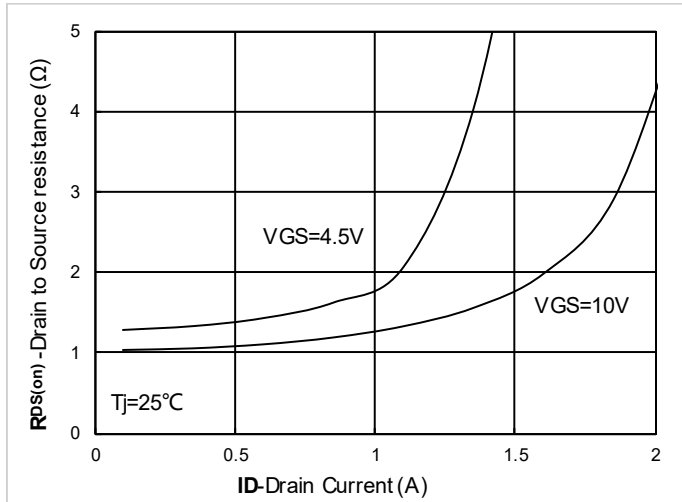


Figure 7.  $R_{DS(on)}$  VS Drain Current

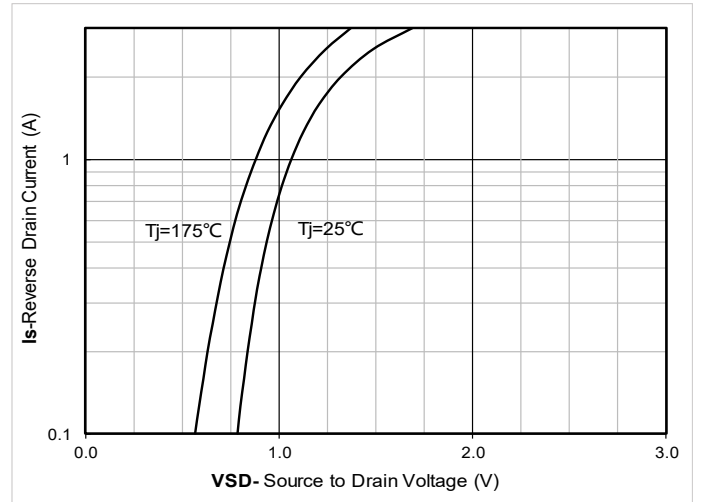


Figure 8. Forward characteristics of reverse diode

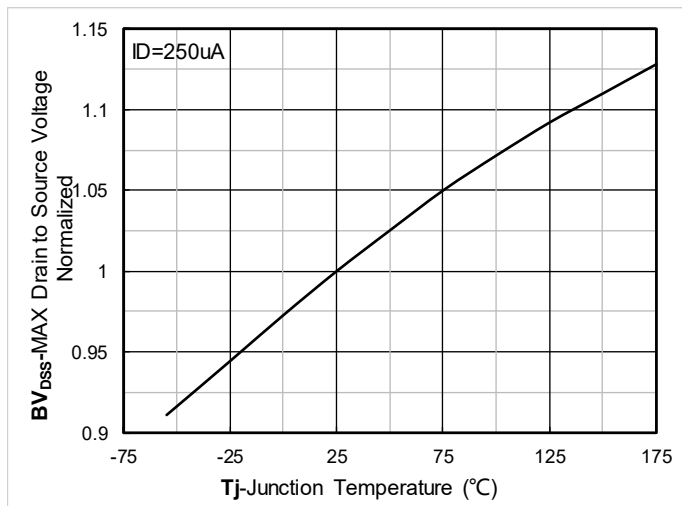


Figure 9. Normalized breakdown voltage

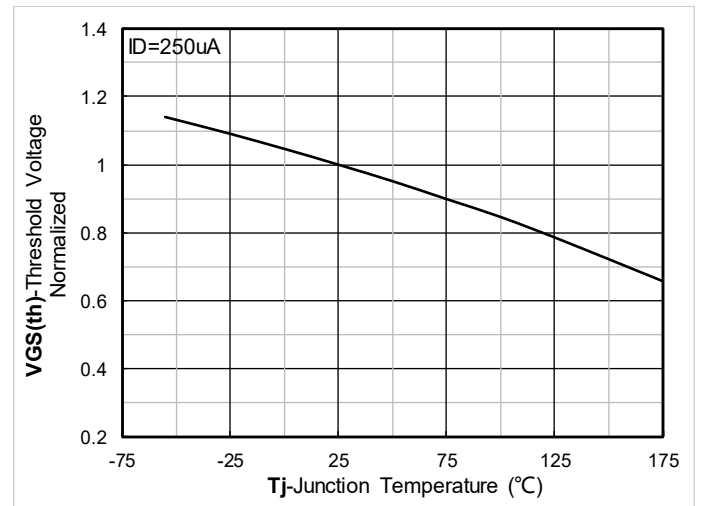


Figure 10. Normalized Threshold voltage

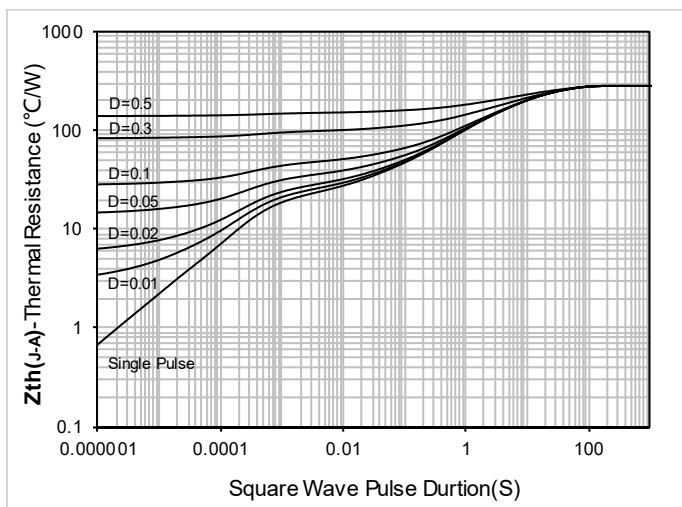


Figure 11. Maximum Transient Thermal Impedance

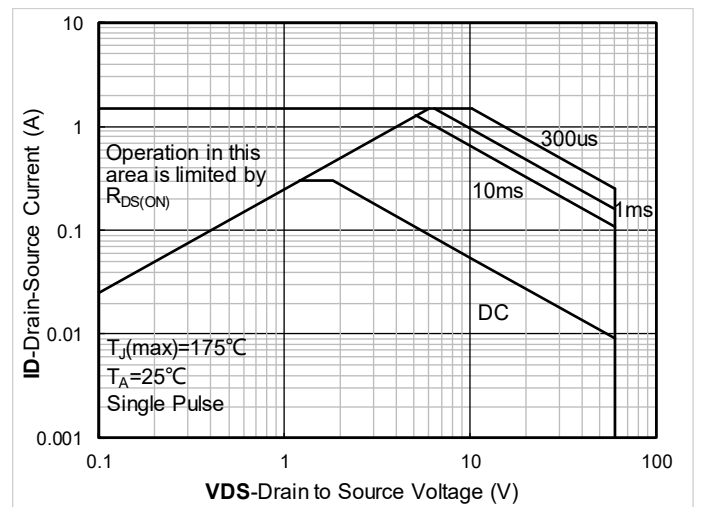


Figure 12. Safe Operation Area

## ■ Test Circuits & Waveforms

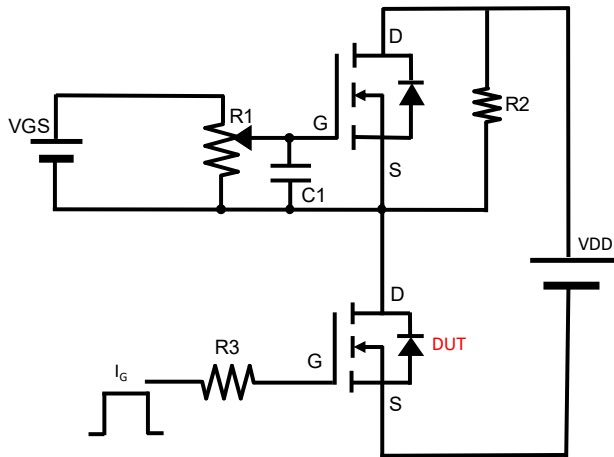


Figure A. Gate Charge Test Circuit & Waveform

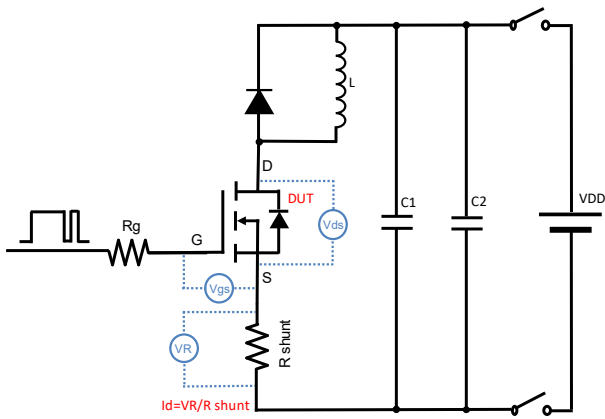


Figure B. Resistive Switching Test Circuit & Waveform

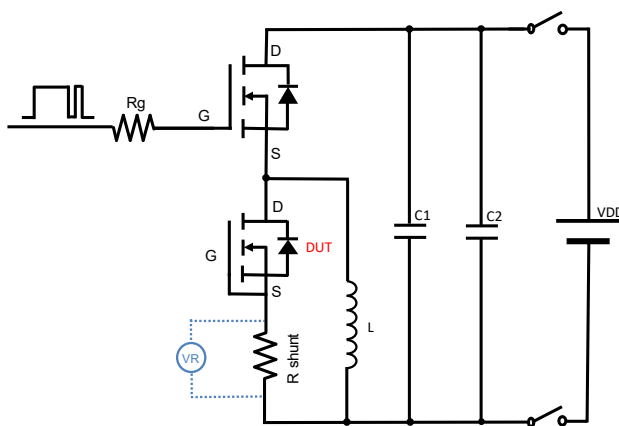
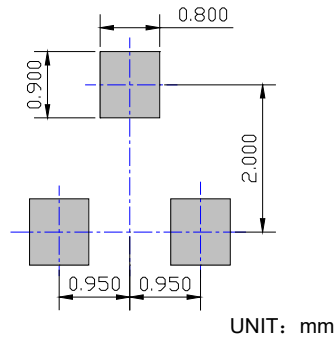
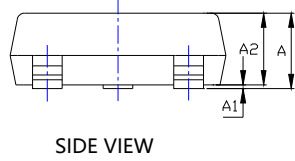
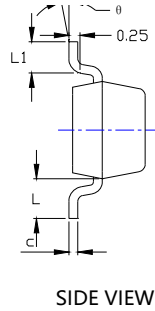
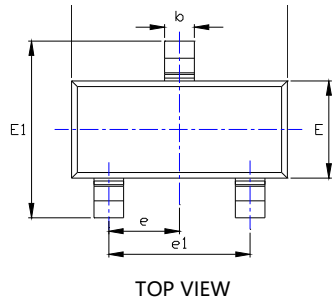


Figure C. Diode Recovery Test Circuit & Waveform



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## ■ SOT-23 Package Outline Dimensions

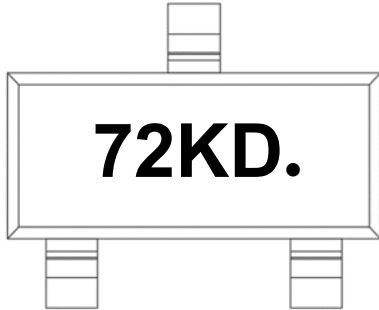


SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

## ■ Marking Information



- Note:
1. All marking is at middle of the product body
  2. All marking is in laser marking
  3. 72KD is Marking Code
  4. Body color: Black



## 2N7002KDHQ

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### Disclaimer

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