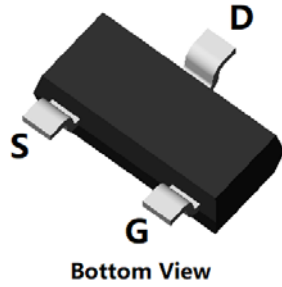
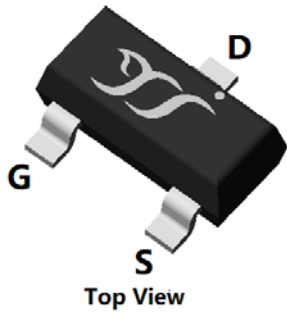
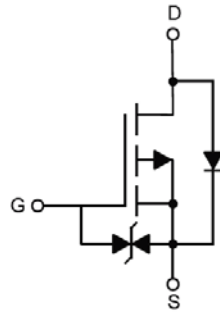


## P-Channel Enhancement Mode Field Effect Transistor



**SOT-23**



### Product Summary

- $V_{DS}$  -20 V
- $I_D$  - 3.9A
- $R_{DS(ON)}$  ( at  $V_{GS}=-4.5V$ ) < 45 m $\Omega$
- $R_{DS(ON)}$  ( at  $V_{GS}=-2.5V$ ) < 75 m $\Omega$
- ESD Protected Up to 2.0KV (HBM)

### General Description

- Split gate trench MOSFET technology
- Low  $R_{DS(on)}$  & FOM
- Extremely low switching loss
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Part no. with suffix "Q" means AEC-Q101 qualified
- Halogen Free

### Applications

- Power management
- Portable equipment

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	-20	V
Gate-source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current	$I_D$	$T_A=25^\circ\text{C}$	-3.9
		$T_A=100^\circ\text{C}$	-2.4
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-23	A
Total Power Dissipation <sup>C</sup>	$P_D$	$T_A=25^\circ\text{C}$	1
		$T_A=100^\circ\text{C}$	0.4
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$R_{\theta JA}$	100	120	$^\circ\text{C/W}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3415KCQ	F2	3415C	3000	30000	120000	7" reel



# YJL3415KCQ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V	-	-	-1	μA
		V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	-100	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V	-	-	±10	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.5	-0.85	-1.25	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3.9A	-	28	45	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2A	-	50	75	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-3.9A, V <sub>GS</sub> =0V	-	-0.9	-1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz, Open drain	-	17	-	Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHz	-	540	-	pF
Output Capacitance	C <sub>oss</sub>		-	120	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	100	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-5A	-	13	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	2	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-5A, di/dt=100A/us	-	2.5	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	20	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-10V, I <sub>D</sub> =-5A R <sub>GEN</sub> =2.2Ω	-	5	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	47	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	52	-	
Turn-off fall Time	t <sub>f</sub>		-	69	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P<sub>d</sub> is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

C. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub> =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



## Typical Electrical and Thermal Characteristics Diagrams

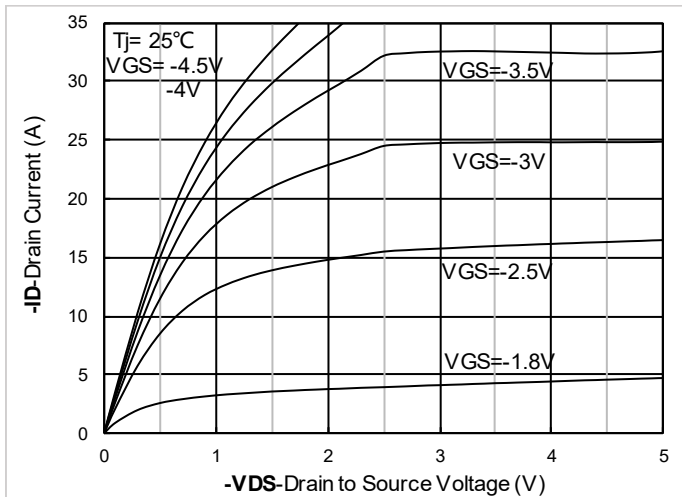


Figure 1. Output Characteristics

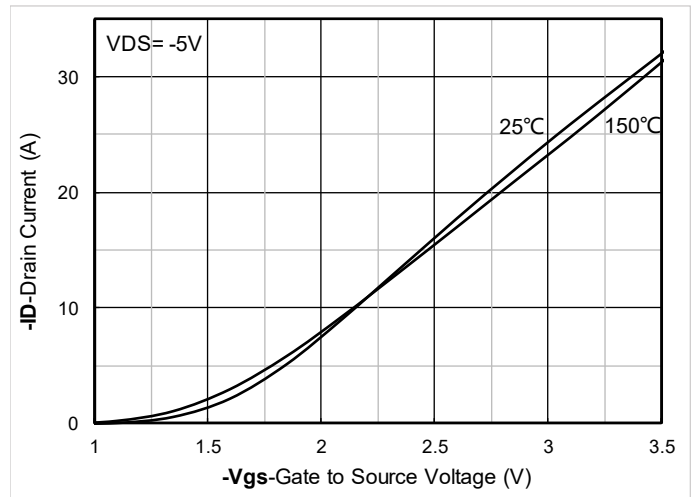


Figure 2. Transfer Characteristics

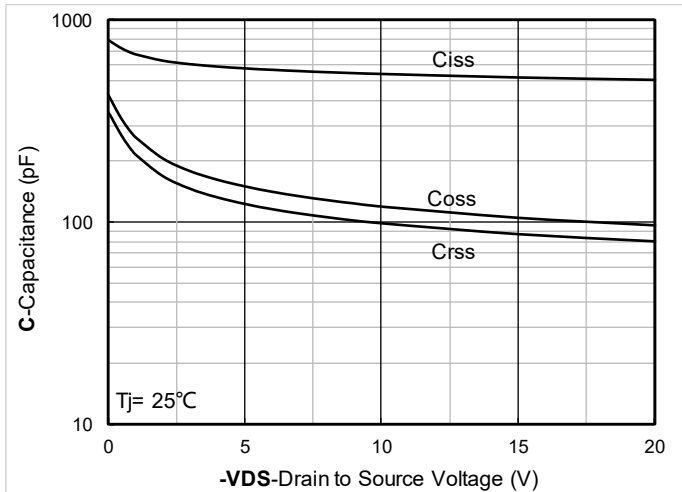


Figure 3. Capacitance Characteristics

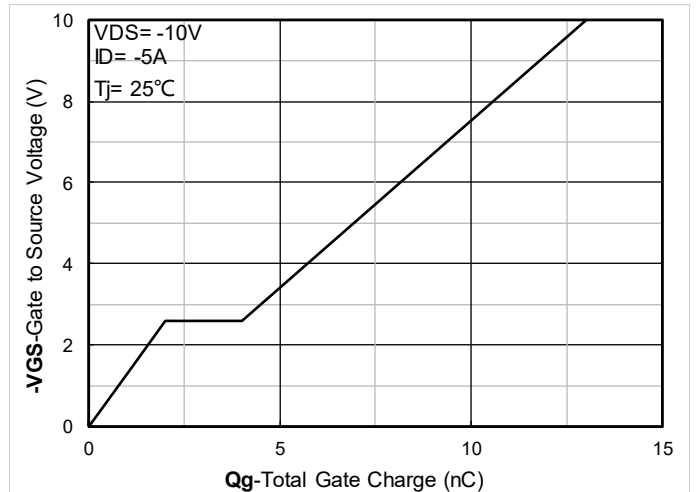


Figure 4. Gate Charge

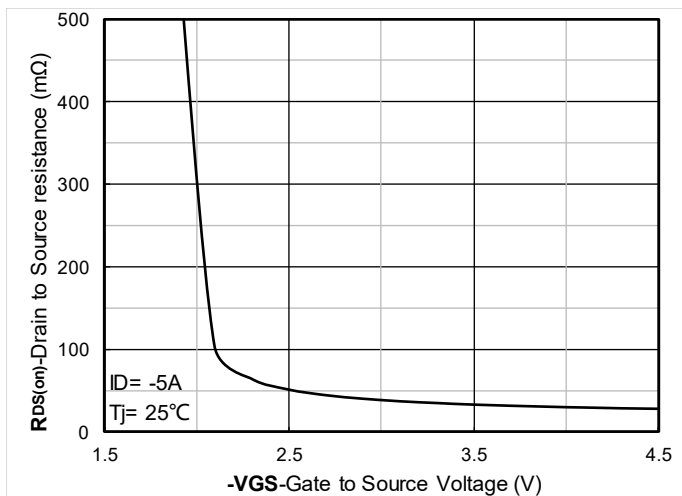


Figure 5. On-Resistance vs Gate to Source Voltage

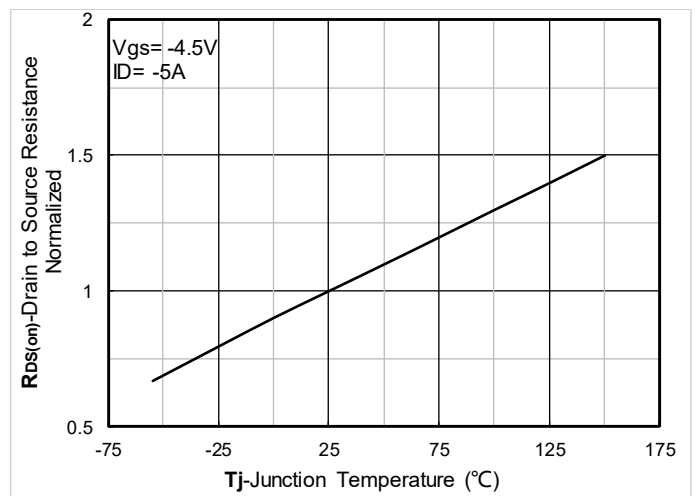


Figure 6. Normalized On-Resistance



# YJL3415KCQ

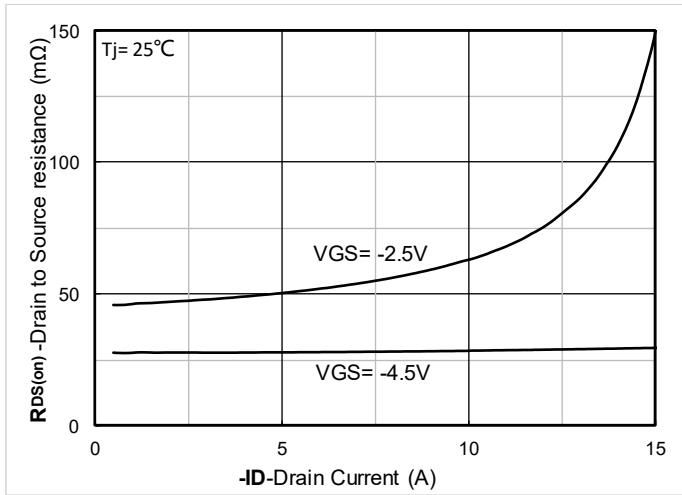


Figure 7.  $R_{DS(on)}$  VS Drain Current

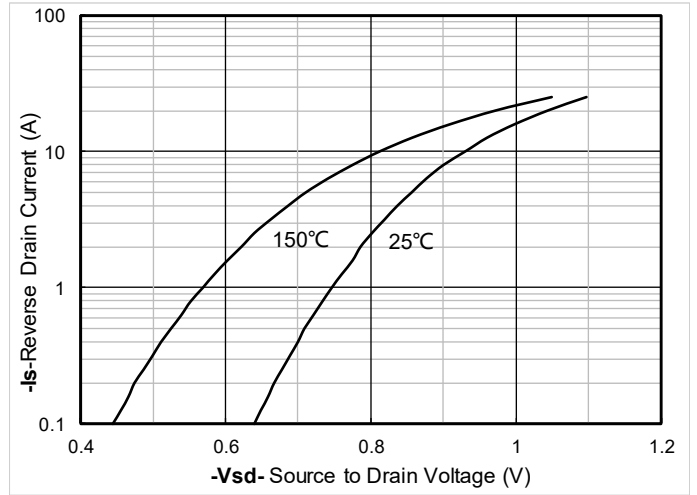


Figure 8. Forward characteristics of reverse diode

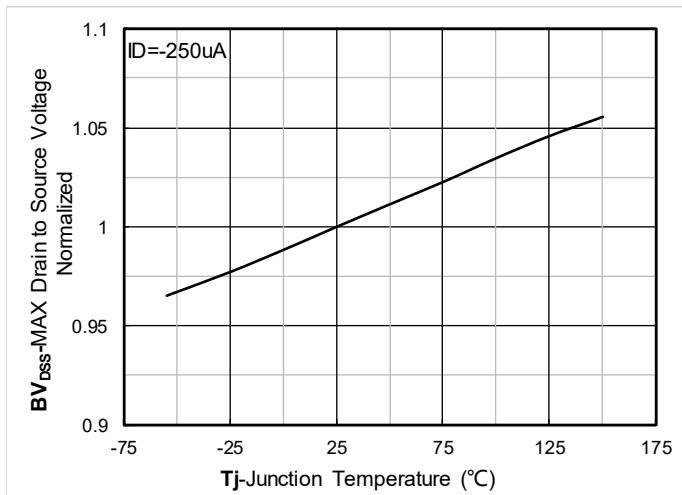


Figure 9. Normalized breakdown voltage

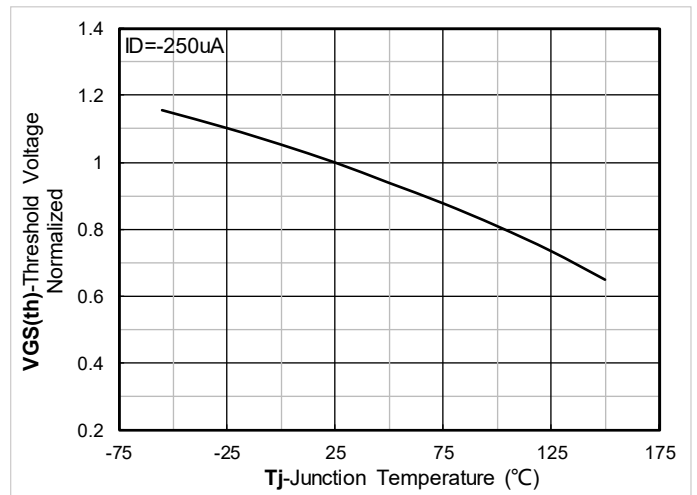


Figure 10. Normalized Threshold voltage

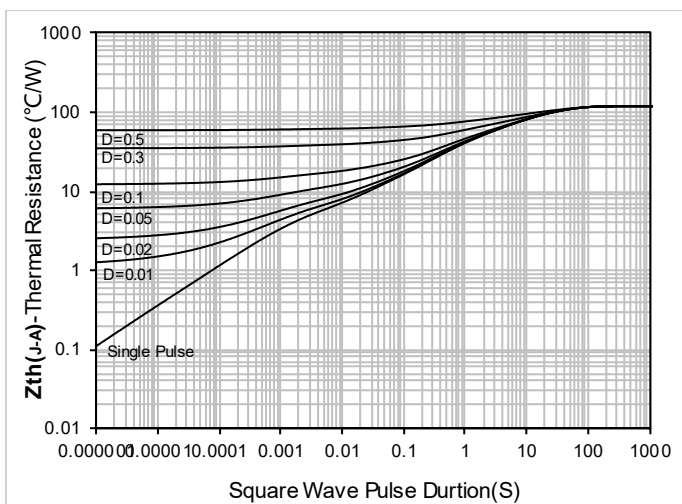


Figure 11. Maximum Transient Thermal Impedance

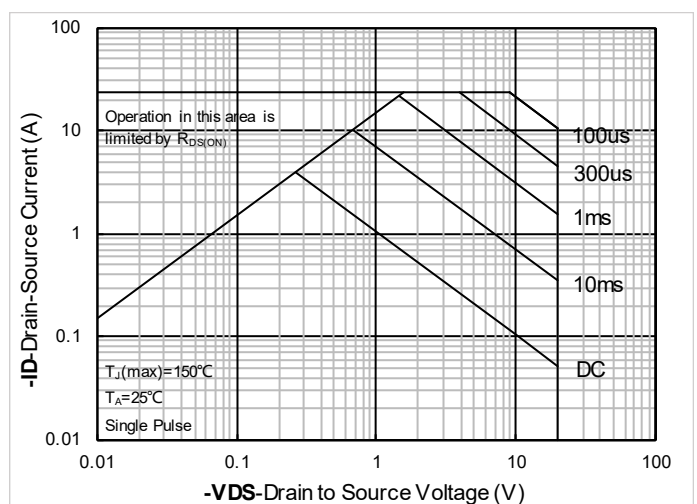
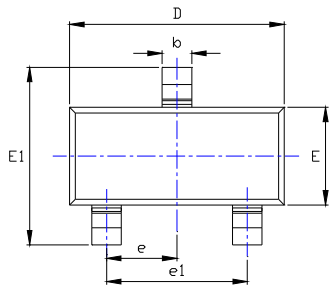


Figure 12. Safe Operation Area

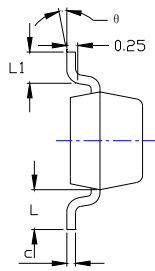


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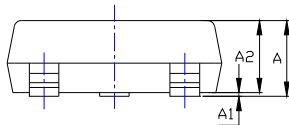
## ■ SOT-23 Package information



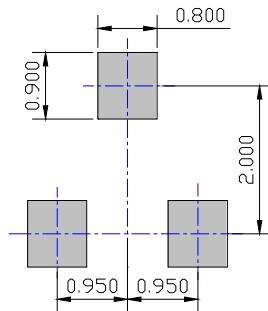
TOP VIEW



SIDE VIEW



SIDE VIEW



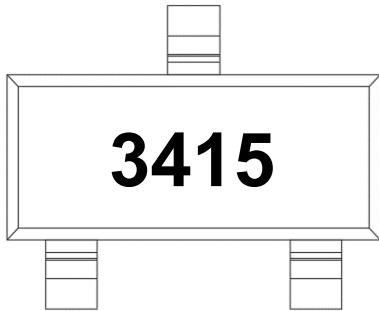
UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:  
 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

## ■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser marking
3. 3415 is Marking Code
4. Body color: Black



## YJL3415KCQ

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